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RESPONSE UNDER 37 C.F.R. 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2143

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Pradeep Sindhu; Dennis C. Ferguson	Confirmation No.	4412
Serial No.:	10/004,536		
Filed:	October 31, 2001	Customer No.:	28863
Examiner:	Joseph E. Avellino		
Group Art Unit:	2143		
Docket No.:	1014-014US01/JNP-0074		
Title:	NETWORK ROUTER HAVING EMBEDDED MEMORY		

CERTIFICATE UNDER 37 CFR 1.8: I hereby certify that this correspondence is being deposited with the United States Post Service, as First Class Mail, in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450 on September 30, 2005.

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants respectfully request a Pre-Appeal Brief Request for Review, based upon the Examiner's failure to establish a prima facie case of obviousness under 35 U.S.C. § 103. Claims 1-9, 11-33 and 34-35 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680). As outlined in greater detail below, the applied references fail to teach or suggest one or more claimed elements. Moreover, the modifications proposed by the Examiner change the principle operation of Mathur, which is

impermissible.[1] For at least these reasons, Applicants request that the obviousness rejections under 35 U.S.C. § 103 be reversed.

For purposes of this request, Applicants have primarily focused the arguments below on pending independent claim 1. By setting forth these clear grounds for error, Applicants do not assert that these are the only errors that the Examiner has made, nor do Applicants waive any arguments that may be asserted in an Appeal Brief.

Applicants' claim 1 requires a routing component that includes an embedded memory within an integrated circuit to buffer data communicated in a first direction from a first interface to a second interface. Thus, an embedded memory internal to the routing component is used to buffer data flowing in the first direction between the interfaces. Claim 1 further requires the routing component to include a memory interface to couple the integrated circuit to an external memory for buffering data communicated in a second direction from the second interface to the first interface. Thus, claim 1 requires the use of an external memory to buffer data flowing in the opposite direction between the same two interfaces. In other words, Applicants' claim 1 requires that different buffering techniques are used for data flowing between the same two interfaces depending upon the direction of the data.

The practicality of this non-obvious technique is set forth in the present application. For example, pg. 6, ll. 8-16 of the present application states:

> In the scalable router arrangement, data communicated from a faster interface to a slower interface is stored in an external memory associated with the routing component that received the data. Thus, for example, data received via the crossbar arrangement is buffered in the external memory before being output via a WAN interface. Data communicated from the WAN interface to the crossbar arrangement [i.e., the opposite direction], on the other hand, is stored in an embedded memory device. ...

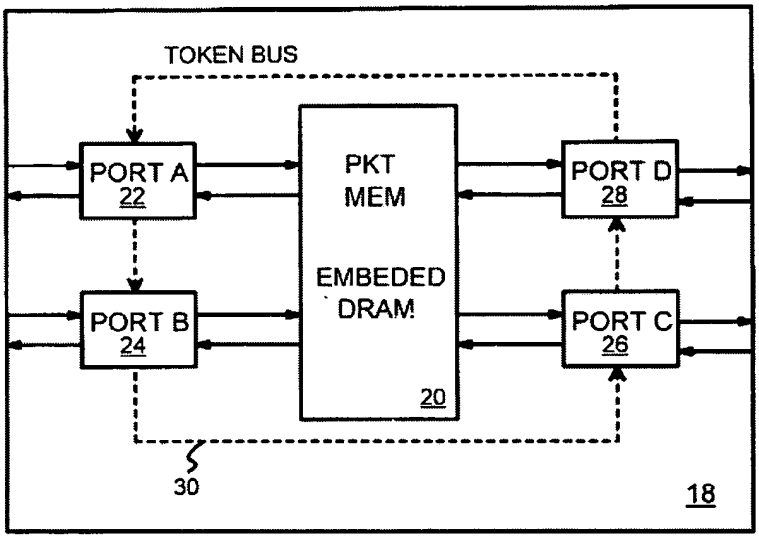
Thus, as illustrated by this example, the described routing architecture may utilize an internal embedded memory when forwarding data from a slower interface (e.g., a WAN interface) to a faster interface (e.g., a switch fabric). However, the same routing component may use an external memory when forwarding data in an opposite direction from the faster interface to the slower interface. This architecture may have certain advantages. For example, interconnect pins of the integrated circuit that may otherwise be used for buffering traffic in a lower bandwidth direction may be avoided by selective use of embedded memory. Moreover, additional pins may instead be

[1] See, e.g., MPEP 2143.01.

used on the integrated circuit to allow utilization of a larger external memory for buffering traffic flowing between the same interfaces but in a higher bandwidth direction. Thus, the integrated circuit may simultaneously use a larger external memory and a high-speed internal memory to achieve advantages in both directions of the data flow.

Mathur (USPN 6,424,658)

Mathur describes a store-and-forward network switch that exclusively uses an embedded dynamic-random-access memory (DRAM) packet memory. In particular, FIG. 2 of Mathur shows a network switch chip 18 that receives packets from one of four ports A, B, C, D and stores the packets in embedded DRAM packet memory 20 for transmission between the ports, as illustrated in the following reproduction of FIG. 2 from Mathur.



Mathur makes clear that packets forwarded in any direction between ports 22-28 are stored in embedded packet memory 20.[2] Thus, Mathur teaches a switch in which packets forwarded between any of the four interface ports 22-26 are buffered within an embedded packet memory 20 regardless of the forwarding direction.

Muller et al. (USPN 6,246,680)

Muller describes a highly integrated multi-layer switch element. According to Muller, the switch element includes multiple ports for transmitting and receiving packets over a network. FIG. 2 of Muller illustrates the described switch element:

[2] See, e.g., col. 6, ll. 3-7 (stating that port logic 22, 24, 26, 28 are bi-directional ports and that when a packet is received by any of the port logics, the packet is written into embedded DRAM packet memory).

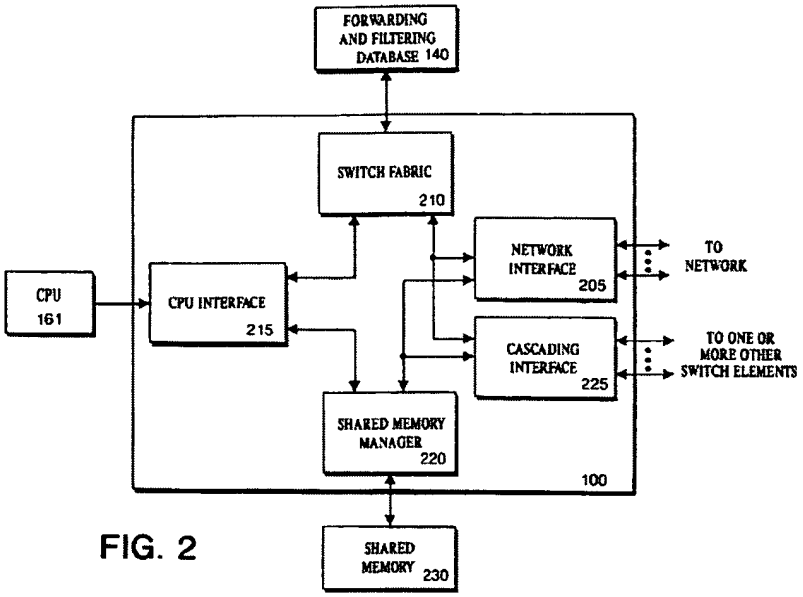


FIG. 2

Muller teaches the exclusive use of an external shared memory 230 for buffering packets flowing between any of the network interfaces 205. At col. 1, ll. 41-60, Muller states that packets are processed by "transferring the incoming packet data to the shared memory manager 220 for temporary storage in an external shared memory 230." Thus, Muller teaches a switch in which an external shared memory 230 is used to buffer packets flowing in between network interfaces 205 regardless of direction. Applicants request reversal of the current rejection under 35 U.S.C. 103 for at least the following reasons.

First, neither Mathur nor Muller, either singularly or in combination, teach or suggest utilization of different buffering techniques between the same interfaces depending on the direction of the data flow. As demonstrated above, Mathur specifically teaches the use of an embedded memory for buffering all data regardless of direction. Muller teaches use of a shared memory for buffering data regardless of direction. Thus, neither Mathur nor Muller, either singularly or in combination, provide a suggestion of a routing component that utilizes different buffering techniques between the same two network interfaces depending on the direction of the data flow, as required by claim 1. Quite contrary to this approach, both Mathur and Muller teach utilization of the same buffering scheme regardless of the direction of the packet flow. In the case of Mathur, an embedded memory is used for all directions. In the case of Mathur, a shared memory is used for all directions. Even when viewed in combination, the references fail to provide a teaching or suggestion of a routing component that utilizes different buffering schemes

when forwarding packets in opposite directions between the same two interfaces, as required by claim 1.

In rejecting claim 1, the Examiner argues that it would be obvious to one skilled in the art to replace the embedded memory of the Mathur switch with the external memory of Muller switch. If one of ordinary skill were to replace the embedded memory of Mathur with the external memory architecture taught by Muller, as suggested by the Examiner, then presumably the modified switch element would use external memory to buffer data in both directions, as specifically taught by Muller. There is no teaching in the references to utilize both an embedded memory and an external memory. Moreover, there is no teaching to selectively use different buffering architectures based on the direction of data flow between the two interfaces. Nowhere does Mathur or Muller, either singularly or in combination, teach or suggest use of embedded and external memories in the manner claimed by the Applicants.

Moreover, modification to Muller to utilize external memories as proposed by the Examiner is directly contrary to the express statements of Muller and would change the principle operation of Mathur, which is impermissible.[3] Muller expressly states that the embedded memory have been utilized to avoid numerous problems associated with external memories.[4]

Applicants request a review and a panel decision that promptly resolves the issues in Applicants' favor and eliminates the need for an Appellate Brief. Please charge any additional fees or credit any overpayment to deposit account number 50-1778. The Examiner is invited to telephone the below-signed attorney to discuss this application.

Date: September 30, 2005

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[3] See, e.g., MPEP 2143.01.
[4] See, e.g., col. 12, ll. 25-65.